Room Temperature Negative Differential Resistance with High Peak-to-Valley Current Ratio of CdF_2/CaF_2 Resonant Tunneling Diode on Silicon

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We have demonstrated room temperature negative differential resistance with high peak-to-valley ratio of nearly 10^6 using CdF_2/CaF_2 double barrier resonant tunneling diode (DBRTD) structures grown on Si(111) substrate. Fluctuation of layer thickness is evaluated at ±1TL (tri-layer=0.31nm) for each layer. The I-V curves are reasonably changed by the layer thickness of CdF_2 quantum-well.

CdF_2/CaF_2 heterostructure is an attractive candidate for quantum device applications on Si substrate such as resonant tunneling diodes (RTD) [1,2] and quantum intersubband transition devices because of the large conduction band discontinuity (ΔE_C~2.9eV) at the heterointerface. Due to the large ΔE_C, RTD using CdF_2/CaF_2 heterostructures are expected to exhibit negative differential resistance (NDR) with high peak-to-valley ratio (PVR) even at room temperature since valley current can be suppressed to low level.

Figure 1 shows the double barrier resonant tunneling diode structure fabricated in this study. Electrons are injected from n+-Si(111) substrate and tunnel through CdF_2 quantum well layer sandwiched by 1nm-thick CaF_2 energy barriers. CaF_2 and CdF_2 epitaxial heterostructures were grown by molecular beam epitaxy (MBE) combined with partially ionized beam of CaF_2 to enhance surface coverage and to obtain atomically flat CaF_2 layers.

After the growth, Au/Al electrode was formed for I-V measurement. In the measurement of current-voltage characteristics at room temperature, clear negative differential resistance (NDR) were obtained. Figure 2 shows current-voltage characteristics of RTD with 100μm×100μm square electrode with CdF_2 quantum-well layer thickness of (a) 3.7nm and (b) 6.5nm. Peak current voltage (V_{peak}) shift was demonstrated and multi-peak characteristics were obtained for RTD as shown in Fig.2 (b). These I-V curves are well fitted by theoretical analysis using Esaki-Tsu formula assuming parasitic serial resistance. Figure 3 shows examples of high peak-to-valley current ratio (PVR) characteristics: (a) PVR=10^6 and (b) PVR=10^5. with electrode of 18μm-diameter. The measured peak current and PVR value agreed well with theory. Dispersion of bias voltage giving the peak current (V_{peak}) was shown in Fig.4, which indicates layer thickness fluctuation was around ±1TL (tri-layer: 0.31nm) of the CdF_2 Q-well layer. The I-V characteristics were reasonably changed by the layer thickness of CdF_2 quantum well.

References:

[1] A. Izumi, N. Matsubara, Y. Kushida, K. Tsutsui, and N. S. Sokolov: Jpn. J. Appl. Phys., **36** (1997) 1849.

[2] M. Watanabe, T. Funayama, T. Teraji, N. Sakamaki, Jpn. J. Appl. Phys., **39** [7B] (2000) L716.

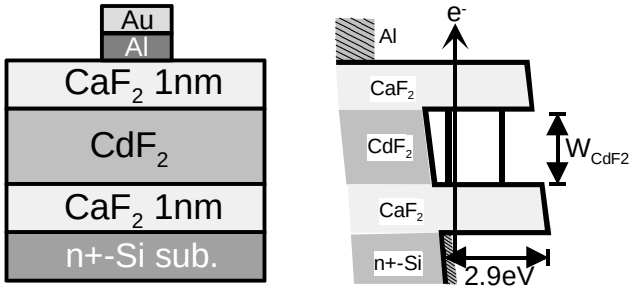

Fig.1 Schematic structure and band diagram of CdF_2/CaF_2 double barrier resonant tunneling diode grown on Si(111) substrate. ΔE_C between CdF_2-CaF_2 is 2.9eV.

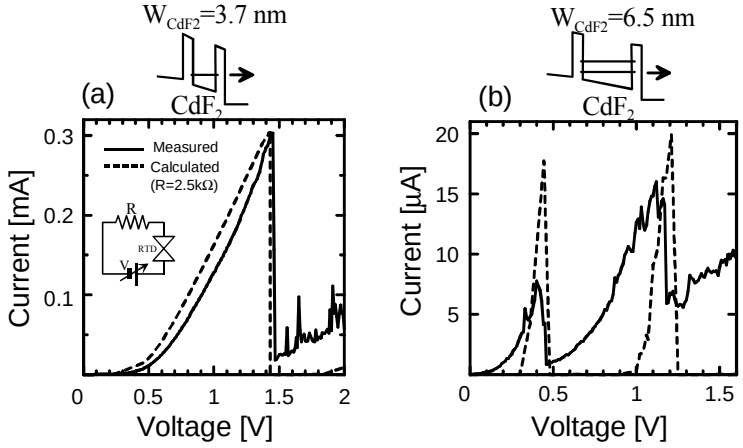

Fig.2 Room temperature I-V characteristics of RTD with different CdF_2 QW-thickness of (a) 3.7 nm, (b) 6.7 nm, respectively. Doted lines indicate result of fitting simulation using Esaki-Tsu formula.

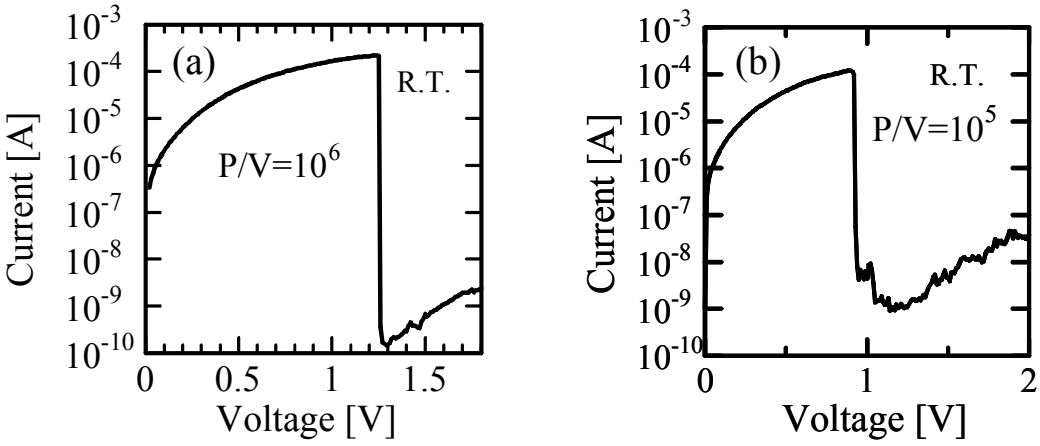

Fig.3 Examples of room temperature I-V characteristics of RTDs with high peak-to-valley ratio (PVR): (a) PVR=10^6, (b) PVR=10^5, respectively.

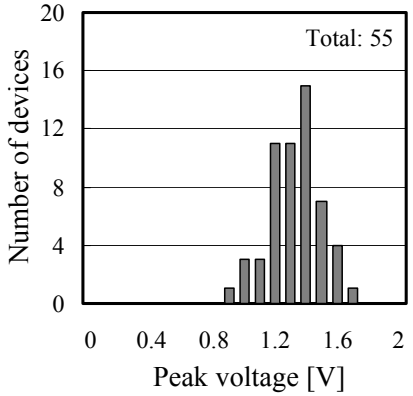

Fig. 4 Histogram of bias voltages for the peak current (V_{peak}) on one wafer. V_{peak} is distributed in the range of 0.7V, which implies that layer thickness fluctuation is around ±1TL (tri-layer: 0.31nm).